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EXAMINER	
MARTINEZ, DAVID E	
ART UNIT	**PAPER NUMBER**
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,347	BOGIN ET AL.	
	Examiner	Art Unit	
	David E. Martinez	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 19-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regards to claim 19, the term "a first direct memory access controller", which appears twice in lines 2-3 and in line 4, renders the claim indefinite since it's not clear if the claim is reciting two distinct instances of "a first direct memory access controller" or if the second instance should be referring to the first instance.

With regards to claims 20-24, due to their dependency from claim 19, they suffer from the same deficiencies and thus are rejected under the same rationale.

Due to the vagueness and a lack of clear definiteness in the claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 19 and 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,792,481 to Hoang et al. (hereinafter Hoang) in view of US Patent No.

6,418,489 to Mason et al. (hereinafter Mason) and further in view of US Patent No. 7,051,123 to Baker et al. (hereinafter Baker).

1. With regards to claim 1, Hoang teaches in a controller [fig 1 element 20, details shown in fig 2] of a computing device [fig 1 system 10, column 2 lines 19-38], computing device comprising a system memory [fig 1 element 16] and a codec [fig 1 element 32], a method comprising

reading data from a buffer [fig 1 element 16] of the system memory [fig 1 element 16] via a first interface of the controller [fig 2 element 22, column 3 lines 28-39],

transferring the data to the codec via a second interface of the controller [fig 2 element 26, column 3 lines 28-39],

tracking a position in the buffer from which the controller has read the data [fig 2 element 78, column 3 lines 29-32, column 5 lines 45-49],

Hoang teaches writing a value to a direct memory access position-in-buffer (DPIB) structure [fig 2 elements 58 and 78, column 3 lines 21-24, column 4 lines 29-32. Elements 58 and 78 are address pointers (pointers being a 'position-in-buffer structure') storing the memory address value of buffer data] located in the controller (figs 1, 2 - element 20). Hoang teaches all of the above limitations except for writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate the position in the buffer. However, Mason teaches a controller that writes values to the system memory via an interface instead of storing them in internal registers to reduce the amount of internal hardware in the controller and improve efficiency and overall performance [column 2 line 48 to column 3 line 3, column 14 lines 19-31].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Hoang and Mason to write a value to a direct memory access

position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate the position in the buffer to reduce the amount of internal hardware in the controller and improve efficiency and overall performance.

The combination of Hoang and Mason teach all of the above limitations but it silent as to receiving a buffer descriptor list from a buffer descriptor list controller, the buffer descriptor list defining a plurality of buffer segments of a buffer to be read, and the reading data from a buffer via a first interface of the controller step as shown above, based, at least in part on the buffer descriptor list. However, Baker teaches receiving a buffer descriptor list from a buffer descriptor list controller [column 36, lines 3-11], the buffer descriptor list defining a plurality of buffer segments of a buffer to be read [column 17, line 65 to column 18 line 3], and the reading data from a buffer via a first interface of a controller, based, at least in part on the buffer descriptor list [column 18 lines 4-20] for the benefit of flexibly specifying data movements between two end points [column 1 line 66 to column 2 line 4].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hoang, Mason and Baker to receive a buffer descriptor list from a buffer descriptor list controller [column 36, lines 3-11], the buffer descriptor list defining a plurality of buffer segments of a buffer to be read [column 17, line 65 to column 18 line 3], and then reading data from a buffer via a first interface of the controller step as shown above, be based, at least in part on the buffer descriptor list [column 18 lines 4-20] for the benefit of flexibly specifying data movements between two end points [column 1 line 66 to column 2 line 4].

2. With regards to claim 3, Hoang teaches the method of claim 1 further comprising tracking progress of transferring the data to the codec via the second interface [column 3 lines 29-50].

3. With regards to claim 4, Hoang teaches the method of claim 1 wherein reading the data from the buffer comprises reading the data per a buffer descriptor list that defines the buffer [fig 2 elements 50, 52, 70, 72 column 3 line 56 to column 4 line 23].

4. With regards to claim 5, Hoang teaches the method of claim 4 wherein reading the data from the buffer further comprises returning to a start of the buffer in response to reaching an end of the buffer [column 4 lines 24-35].

5. With regards to claim 6, Hoang teaches the method of claim 1 further comprises, prior to writing the value to system memory, determining to update the value in the system memory based upon the data transferred via the second interface [column 4 lines 29-32].

6. With regards to claim 19, Hoang teaches a controller [fig 1 element 20, details shown in fig 2] comprising

a first direct memory access controller [fig 1 element 20, details shown in fig 2] to transfer data between a system memory [fig 1 element 16] and a codec [fig 1 element 32] via a first interface to the system memory [fig 2 element 22, column 3 lines 28-39] and a second interface to the codec [fig 2 element 26, column 3 lines 28-39], and

a position controller [fig 2 elements 56, 76] to update a position value in a direct memory access position-in-buffer (DPIB) structure [fig 2 elements 58 and 78, column 3 lines 21-24, column 4 lines 24-35] indicating progress of the first direct memory access controller transferring data between the system memory and the codec via the first interface [fig 2 elements 58 and 78, column 3 lines 21-24, column 4 lines 29-32. Elements 58 and 78 are address pointers (pointers being a 'position-in-buffer structure') storing the memory address value of buffer data] located in the controller (figs 1, 2 - element 20)]. Hoang teaches all of the above limitations except for the direct memory access position-in-buffer (DPIB) structure being located in the system memory. However, Mason teaches a controller that writes values to the

system memory via an interface instead of storing them in internal registers to reduce the amount of internal hardware in the controller and improve efficiency and overall performance [column 2 line 48 to column 3 line 3, column 14 lines 19-31].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Hoang and Mason to have the direct memory access position-in-buffer (DPIB) structure be located in the system memory rather than inside the controller for the benefit of reducing the amount of internal hardware in the controller and improve efficiency and overall performance.

The combination of Hoang and Mason teach all of the above limitations but it silent as to a buffer descriptor list controller to provide a buffer descriptor list to a first direct memory access controller, and to the step for a first direct memory access controller, as disclosed above, to transfer data between a system memory and a codec via a first interface to the system memory and a second interface to the codec, being based on at least in part, on the buffer descriptor list. However, Baker teaches a buffer descriptor list controller to provide a buffer descriptor list to a first direct memory access controller [column 36, lines 3-11, column 17, line 65 to column 18 line 3], and the transferring of data between two endpoints via a first interface to the first endpoint and a second interface to the second endpoint, being based on at least in part, on the buffer descriptor list [column 18 lines 4-20] for the benefit of flexibly specifying data movements between two end points [column 1 line 66 to column 2 line 4].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hoang, Mason and Baker to have a buffer descriptor list controller to provide a buffer descriptor list to a first direct memory access controller, and to the step for a first direct memory access controller, as disclosed above, to transfer data between a system memory and a codec via a first interface to the system memory and a second interface to the

codec, being based on at least in part, on the buffer descriptor list for the benefit of flexibly specifying data movements between two end points [column 1 line 66 to column 2 line 4].

7. With regards to claim 20, it is of the same scope as claim 4 above, and thus is rejected under the same rationale. Furthermore, Hoang teaches the buffer descriptor list is included in a dma controller [fig 1 and 2 element 20] rather than inside the system memory. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the buffer descriptor list in the system memory for the same reasons as those set forth in the claim 19 rejection above.

Claims 2, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,792,481 to Hoang et al. (hereinafter Hoang) in view of US Patent No. 6,418,489 to Mason et al. (hereinafter Mason) in view of US Patent No. 7,051,123 to Baker et al. (hereinafter Baker). and further in view of Applicant's Admitted Prior Art (hereinafter AAPA).

8. With regards to claim 2, Hoang teaches receiving the data via the first interface [fig 2 element 22, column 3 lines 28-39], but the combination of Hoang and Mason are silent as to wherein reading comprises isochronously receiving the data via the first interface. However, AAPA teaches using isochronous data transfers for the benefit of helping multimedia applications such as audio and video applications achieve high quality results [page 1, paragraph 1].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hoang, Mason and AAPA to isochronously receive the data via the first interface for the benefit of helping multimedia applications such as audio and video applications achieve high quality results.

9. With regards to claim 23, Hoang teaches the first direct memory access controller [fig 1 element 20, details shown in fig 2] writes the data to the buffer [column 5 lines 1-5 and 45-46],

but is silent as to the writing being isochronous. However, isochronous writes (a data transfer) is rejected under AAPA as in claim 2 using the same rationale.

10. With regards to claim 24, Hoang teaches the first direct memory access controller [fig 1 element 20, details shown in fig 2] reads the data from the buffer [column 3 lines 28-39, and column 5 lines 45-46], but is silent as to the reading being isochronous. However, isochronous reads (a data transfer) is rejected under AAPA as in claim 2 using the same rationale.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,792,481 to Hoang et al. (hereinafter Hoang) in view of US Patent No. 6,418,489 to Mason et al. (hereinafter Mason) in view of US Patent No. 7,051,123 to Baker et al. (hereinafter Baker). and further in view of US Patent No. 6,693,753 to Su et al. (hereinafter Su)

11. With regards to claim 21, Hoang teaches the controller of claim 19 having the first direct memory access controller [figs 1, 2 - element 20] transfer data across the second interface [fig 2 element 22 connected to bus element 11], but is silent as to the controller of claim 19 further comprises a link counter to maintain a count indicating progress of the data transfer across the second interface. However, Su teaches using a link position counter in an interface between two communicating devices for the benefit of tracking the progress of the data transfer [column 7 lines 4-22].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hoang, Mason and Su to further comprise a link counter to maintain a count indicating progress of the first direct memory access controller in transferring the data across the second interface for the benefit of tracking the progress of the data transfer.

12. With regards to claim 22, Hoang teaches the controller of claim 19 having the first direct memory access controller [figs 1, 2 - element 20] transfer data across the first interface [fig 2 element 22 connected to bus element 11] but is silent as to the controller of claim 19 further

comprises a buffer position counter to maintain a count indicating the progress of the data transfer across the first interface. However, Su teaches using a buffer position counter in an interface between two communicating devices for the benefit of tracking the progress of the data transfer [column 7 lines 4-22].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hoang, Mason and Su to further comprise a buffer position counter to maintain a count indicating progress of the first direct memory access controller in transferring the data across the second interface for the benefit of tracking the progress of the data transfer.

Response to Arguments

Applicant's arguments with respect to claims 1-7 and 19-24 have been considered but are moot in view of the new ground(s) of rejection.

As per Applicant's arguments directed to combinations of Hoang, Mason, AAPA and the Su references directed to claims 1-7 and 19-24, their deficiencies have been corrected by the addition of the Baker reference to the prior combinations.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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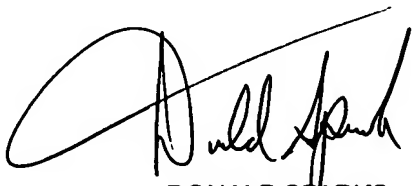

DONALD SPARKS
SUPERVISORY PATENT EXAMINER